Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please cancel claims 6 and 15. Please amend claims 1, 7, 9, and 16, as follows:

Listing of Claims:

1. (Currently amended) A memory system, comprising:

a memory hub controller adapted to provide memory command packets including information to access memory devices;

a memory module having a plurality of memory devices coupled to a memory hub, the memory hub adapted to receive memory command packets and access the memory devices according to the memory command packets and further adapted to provide memory responses in response thereto, the memory hub including

a switch circuit having a plurality of switch nodes and adapted to couple any one switch node to another switch node,

a plurality of link interface circuits, each link interface circuit having a first node coupled to a respective one of the plurality of switch nodes and further having a second node coupled to either the first or second portions of the memory bus, each link interface circuit coupling signals from its first node to its second node,

a memory controller coupled to a switch node of the switch circuit to receive memory command packets and translate the same into memory device command signals, and

a local memory bus coupled to the memory controller and the memory devices on which the memory device command signals are provided;

a first portion of a memory bus coupled to the memory hub controller and the memory hub on which the memory command packets from the memory hub controller are provided to the memory hub of the memory module and memory responses are provided to the memory hub controller;

an expansion module having a processor circuit adapted to provide memory command packets including information to access the memory devices of the memory module and further adapted to process data included in the memory responses from the memory hub; and

a second portion of the memory bus coupled to the memory hub of the memory module and the processor circuit of the expansion module on which the memory command packets from the processor circuit are provided to the memory hub of the memory module and memory responses are provided to the processor circuit.

2. (Original) The memory system of claim 1 wherein the first and second portions of the memory bus comprise:

a downstream bus having a first portion coupled between the memory hub controller and the memory hub to which memory command packets from the memory hub controller to the memory hub are coupled and further having a second portion coupled between the memory hub and the processor circuit to which memory responses from the memory hub to the processor circuit are coupled; and

an upstream bus having a first portion coupled between the memory hub controller and the memory hub to which memory responses from the memory hub to the memory hub controller are coupled and further having a second portion coupled between the memory hub and the processor circuit to which memory command packets from the processor circuit to the memory hub are coupled.

3. (Original) The memory system of claim 1 wherein the expansion module further comprises:

a plurality of memory devices adapted to provide a local memory space; and

a local memory bus coupled to the processor circuit and the plurality of memory devices through which the processor circuit accesses the local memory space.

4. (Original) The memory system of claim 1 wherein the processor circuit of the expansion module comprises a graphics controller to process graphics data stored in the memory devices of the memory module.

5. (Original) The memory system of claim 1 wherein the processor circuit of the expansion module comprises an input/output processor to process input data and store the same in the memory devices of the memory module and to process output data stored in the memory devices of the memory module.

6. (Cancelled)

7. (Currently amended) The memory system of claim 1 [[6]] wherein the plurality of link interface circuits comprise:

a first pair of link interface circuits having a downstream link interface coupled to a first portion of a downstream bus and further having an upstream link interface coupled to a first portion of an upstream bus, both the first portions of the downstream and upstream buses coupled to the memory hub controller and the memory hub; and

a second pair of link interface circuits having a downstream link interface coupled to a second portion of the downstream bus and further having an upstream link interface coupled to a second portion of the upstream bus, both the second portions of the downstream and upstream buses coupled to the memory hub and the processor circuit.

8. (Original) The memory system of claim 1 wherein the memory devices of the memory module comprise synchronous dynamic random access memory devices.

9. (Currently amended) A memory system, comprising:

first and second memory modules, each memory module having a respective plurality of memory devices and a respective memory hub coupled to the respective plurality of memory devices, the respective memory hubs adapted to receive memory requests for accessing

memory locations in the respective plurality of memory devices and provide memory responses in response to receiving the memory requests, the memory hub of at least one of the memory modules including

a switch circuit having a plurality of switch nodes and adapted to couple any one switch node to another switch node,

a plurality of link interface circuits, each link interface circuit having a first node coupled to a respective one of the plurality of switch nodes and further having a second node coupled to the memory bus, each link interface circuit coupling signals from its first node to its second node,

a memory controller coupled to a switch node of the switch circuit to receive memory requests and translate the same into memory device command signals, and

a local memory bus coupled to the memory controller and the memory devices on which the memory device command signals are provided;

first and second expansion modules, each expansion module having a respective processor circuit adapted to provide memory requests to the memory hubs to access memory locations in the respective plurality of memory devices and receive memory responses from the memory hubs;

a memory hub controller adapted to provide memory requests to the memory modules to the memory hubs to access memory locations in the respective plurality of memory devices and receive memory responses from the memory hubs; and

a memory bus coupled to the first and second memory hubs, the first and second processor circuits and the memory hub controller, the memory bus configured to couple memory requests to the memory modules and couple memory responses to the memory hub controller and the first and second processor circuits.

10. (Original) The memory system of claim 9, further comprising a third memory module having a third plurality of memory devices and a third memory hub coupled to the third plurality of memory devices and further coupled to the memory bus in a point-to-point arrangement, the point-to-point arrangement coupling the memory hub controller to the first

memory hub of the first memory module, coupling the first memory hub to the second memory hub of the second memory module, coupling the second memory hub to the first processor circuit of the first expansion module, coupling the first processor circuit to the third memory hub of the third memory module; and coupling the third memory hub to the second processor circuit of the second expansion module.

11. (Original) The memory system of claim 9 wherein the memory bus comprises a pair of unidirectional buses having portions coupled between the first and second memory hubs, the first and second processor circuits and the memory hub controller to provide the point-to-point arrangement.

12. (Original) The memory system of claim 9 wherein at least one of the first and second expansion modules further comprises:

a plurality of memory devices adapted to provide a local memory space; and

a local memory bus coupled to the respective processor circuit and the respective plurality of memory devices through which the processor circuit accesses the local memory space.

13. (Original) The memory system of claim 9 wherein the processor circuit of at least one of the first and second expansion modules comprises a graphics controller to process graphics data stored in the memory devices of at least one of the memory modules.

14. (Original) The memory system of claim 9 wherein the processor circuit of at least one of the first and second expansion modules comprises an input/output processor to process input data and store the same in the memory devices of at least one of the memory modules and to process output data stored in the memory devices of the memory module.

15. (Cancelled)

16. (Currently amended) The memory system of claim 9 [[15]] wherein the memory bus comprises a unidirectional downstream bus and a unidirectional upstream bus, and the plurality of link interface circuits comprise:

a first pair of link interface circuits having a downstream link interface coupled to a first portion of the downstream bus and further having an upstream link interface coupled to a first portion of the upstream bus; and

a second pair of link interface circuits having a downstream link interface coupled to a second portion of the downstream bus and further having an upstream link interface coupled to a second portion of the upstream bus.

17. (Original) The memory system of claim 9 wherein the memory devices of the memory module comprise synchronous dynamic random access memory devices.

18-44. (Cancelled)